

FIG. 1

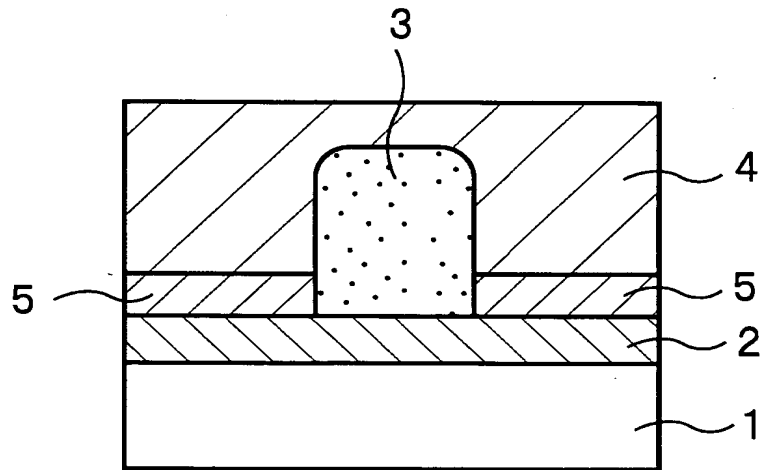


FIG. 2

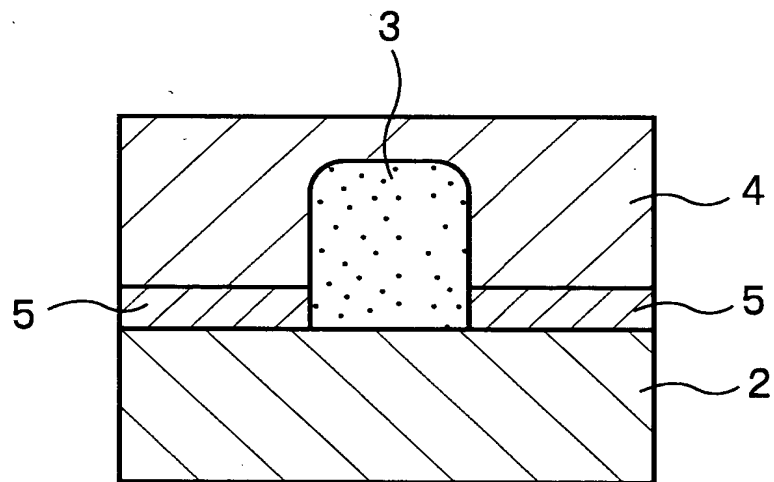


FIG. 3

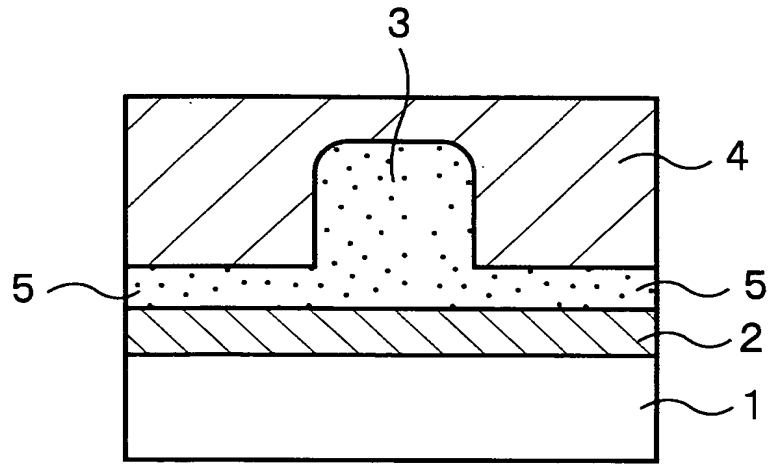


FIG. 4

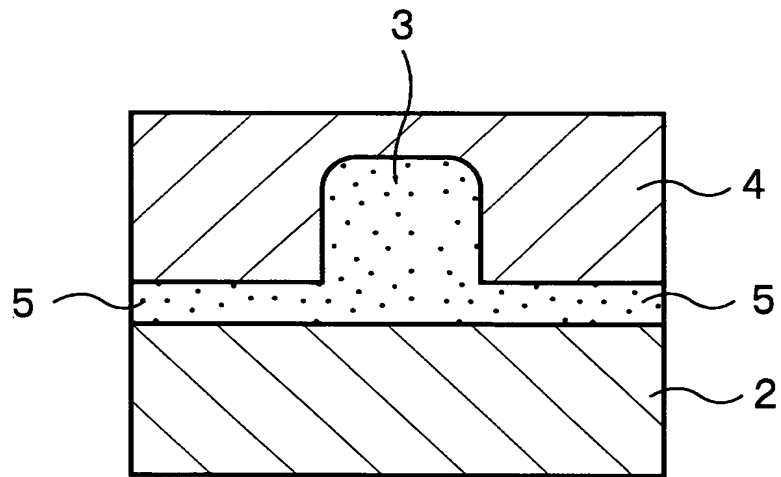


FIG. 5 (a)

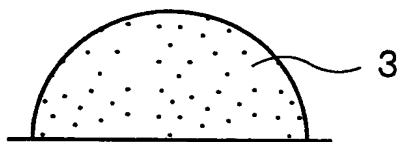


FIG. 5 (b)

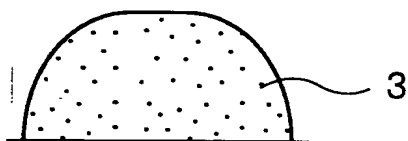


FIG. 5 (c)

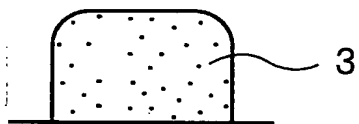


FIG. 5 (d)

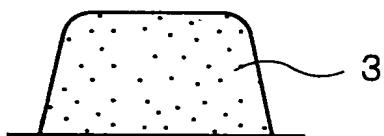


FIG. 5 (e)

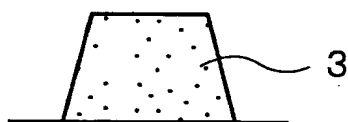


FIG. 5 (f)

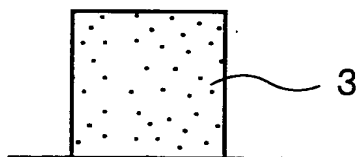


FIG. 6(a)

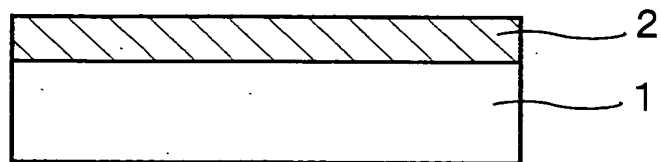


FIG. 6(b)

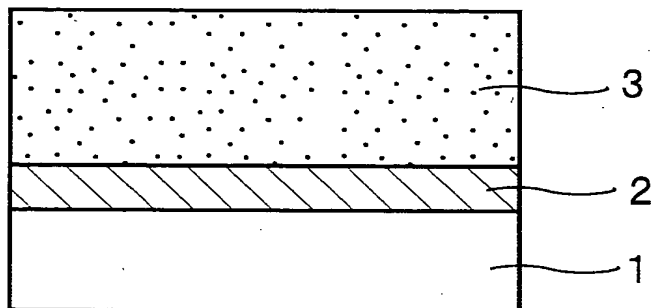


FIG. 6(c)

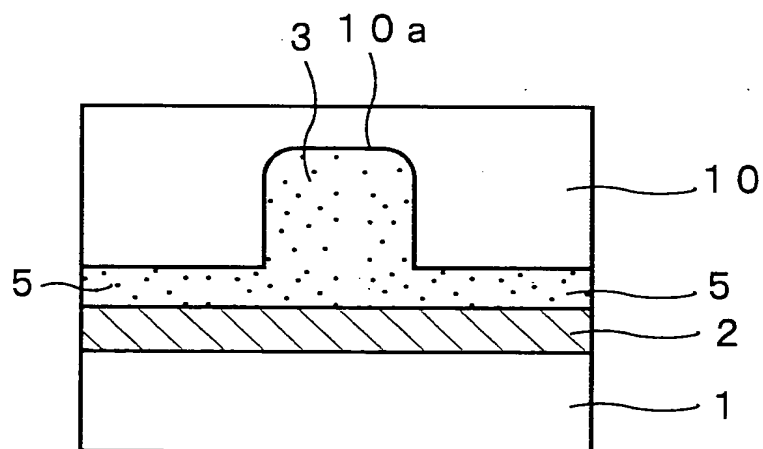


FIG. 7 (d)

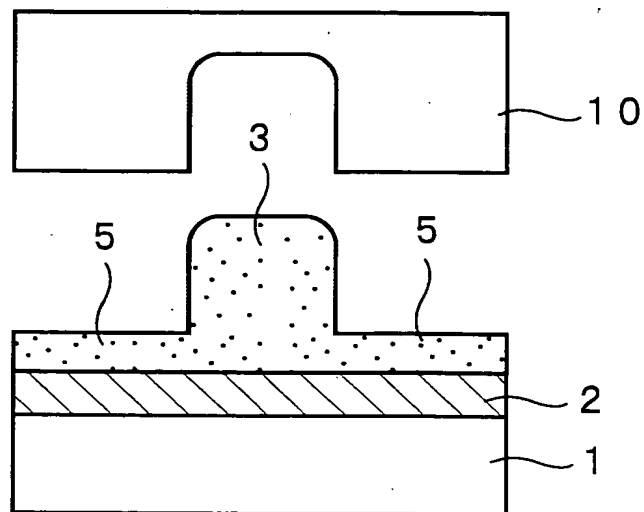


FIG. 7 (e)

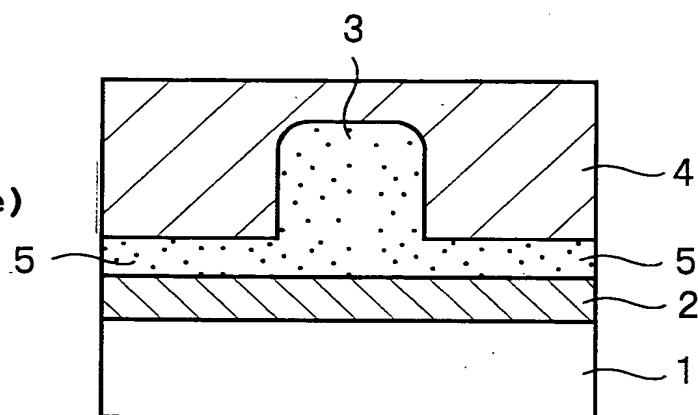


FIG. 8

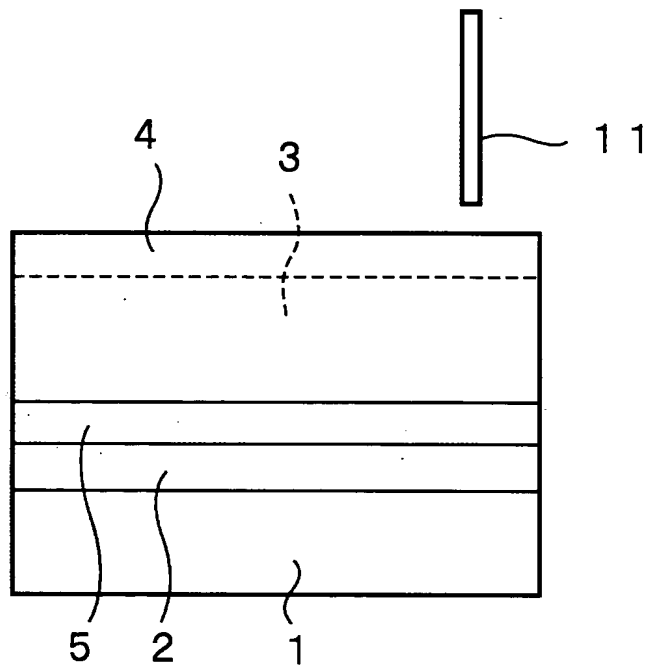


FIG. 9

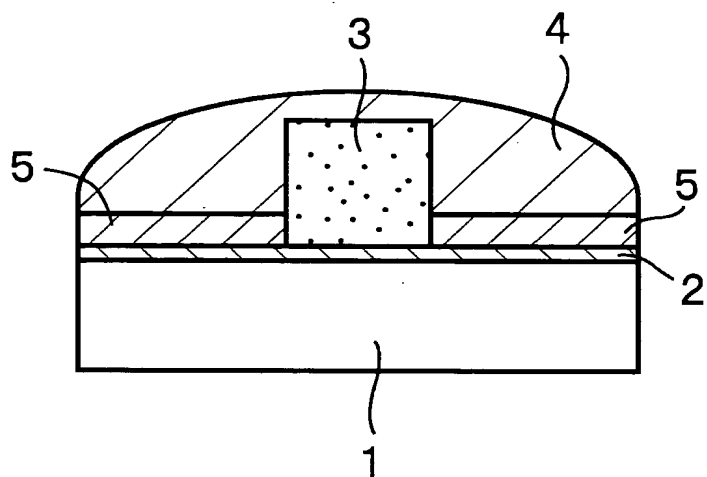


FIG. 10 (a)

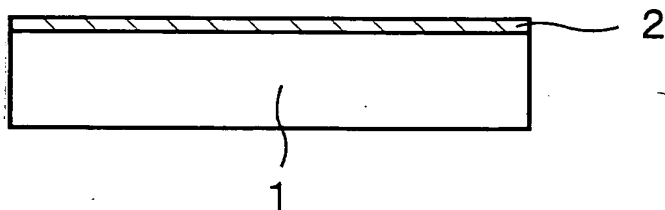


FIG. 10 (b)

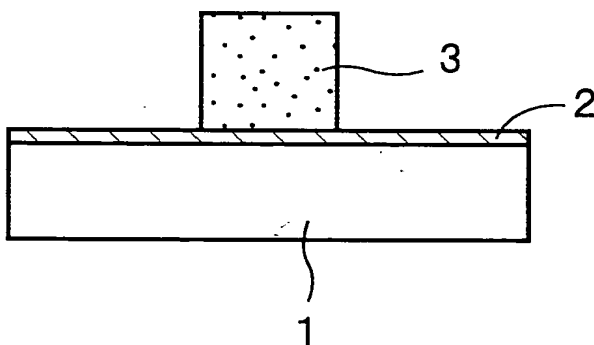


FIG. 10 (c)

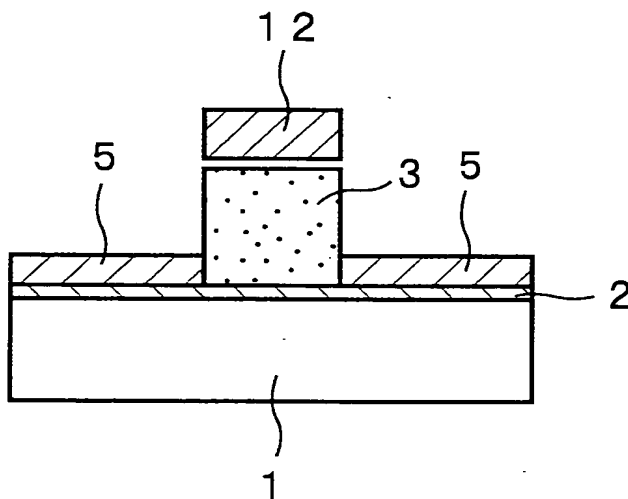


FIG. 11

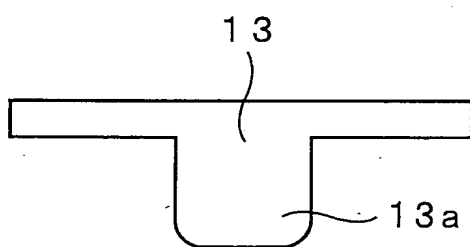
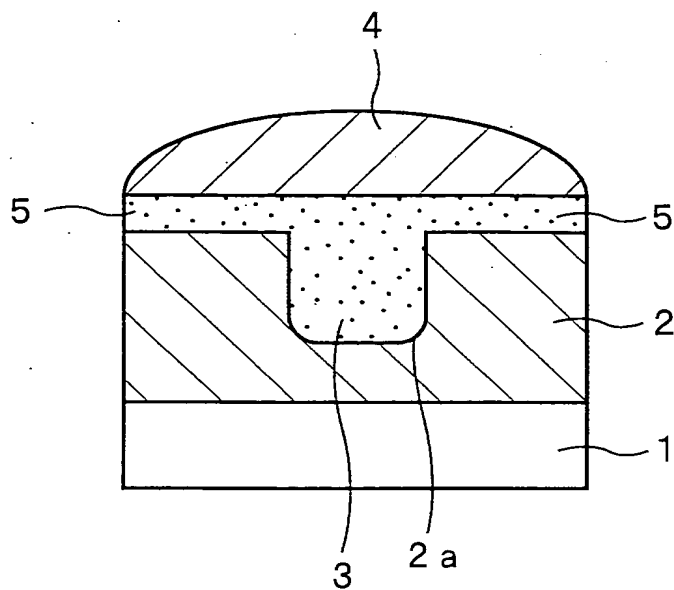


FIG. 12 (a)

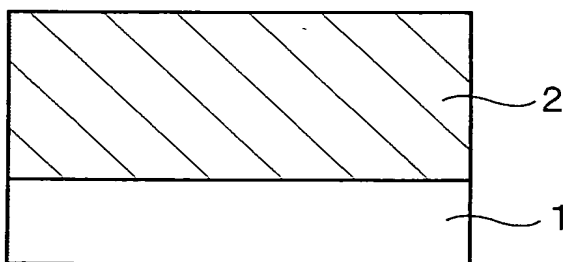
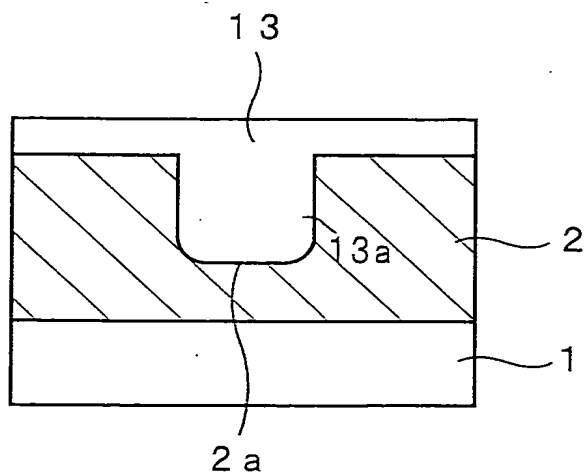


FIG. 12 (b)



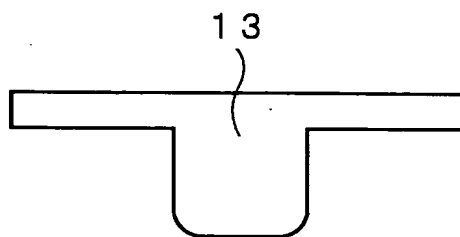


FIG. 13(c)

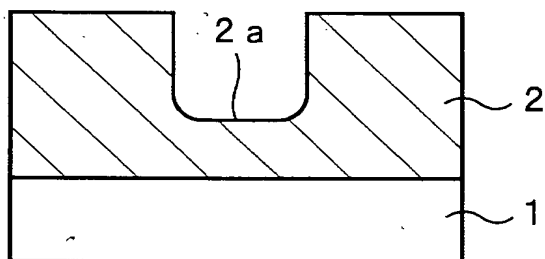


FIG. 13(d)

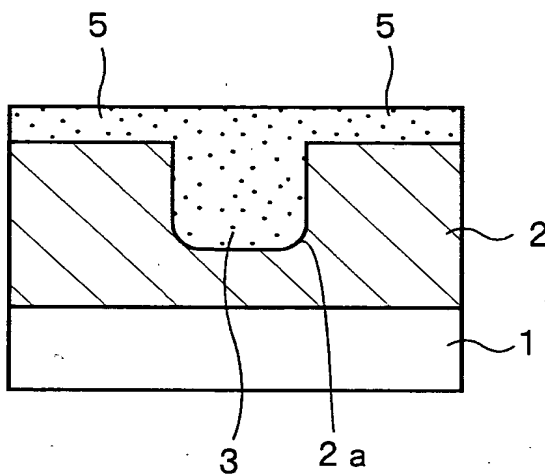
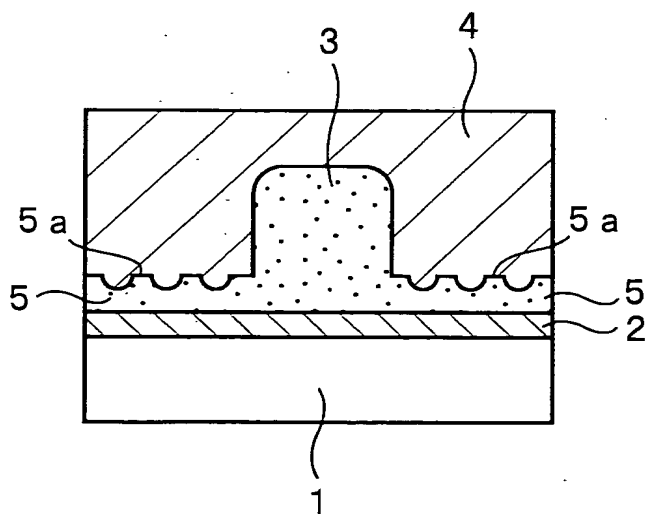


FIG. 14



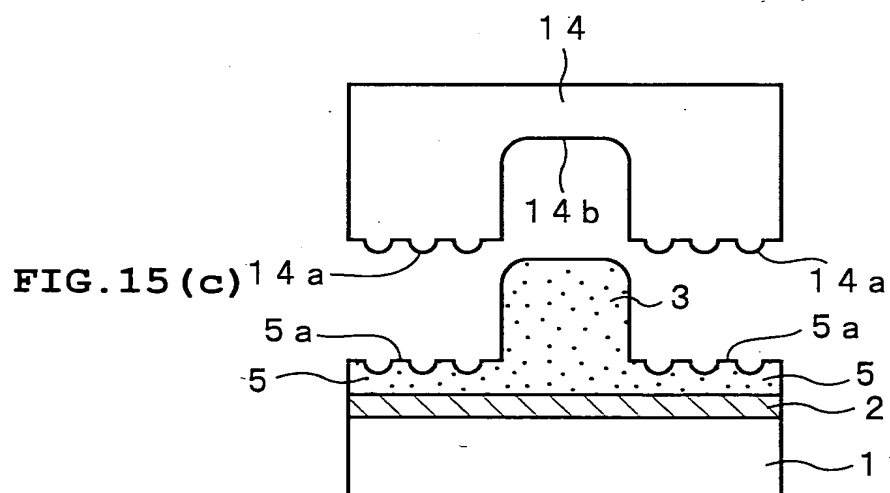
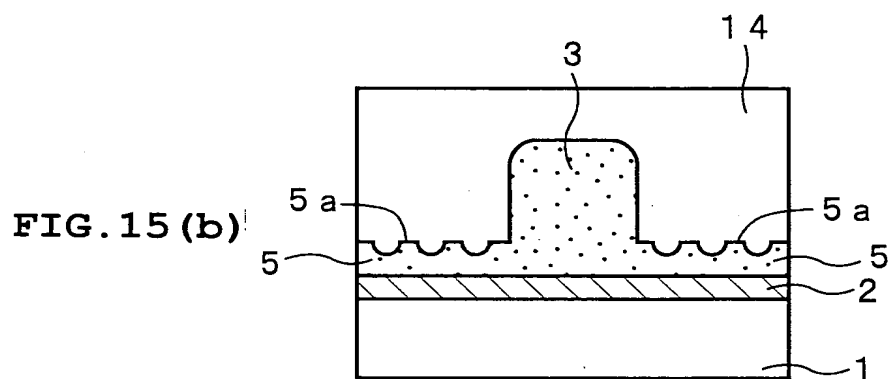
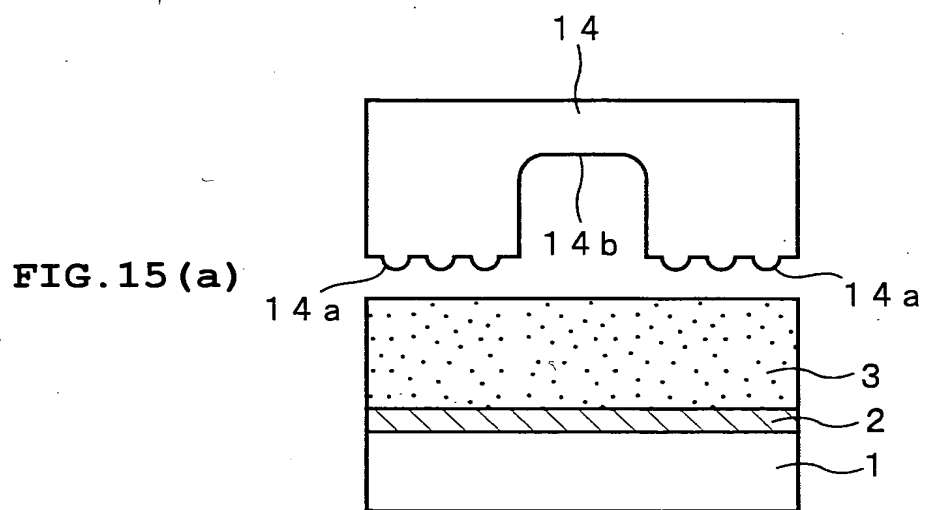
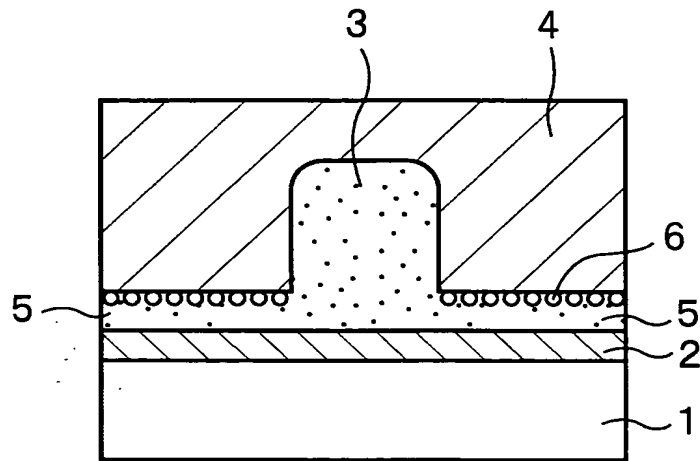


FIG.16



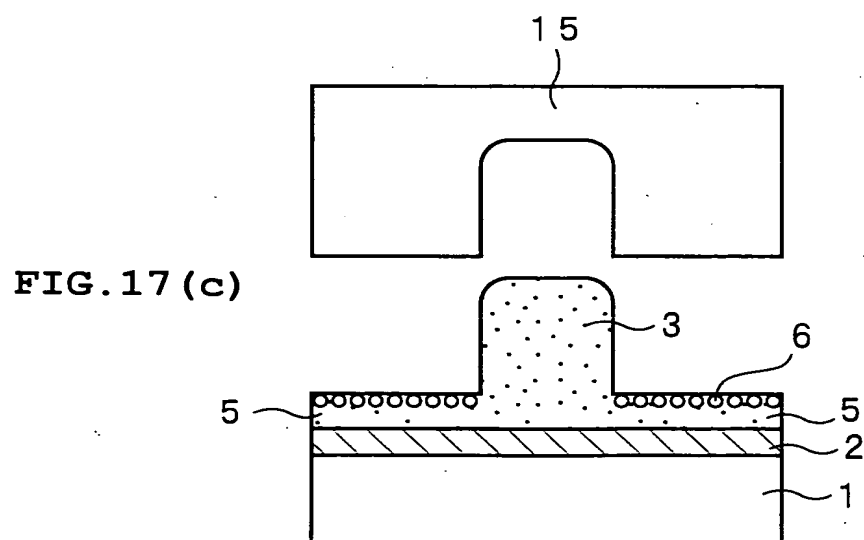
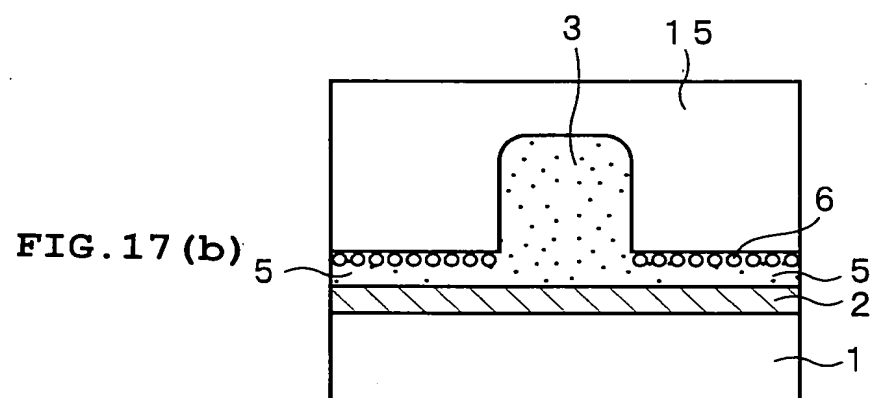
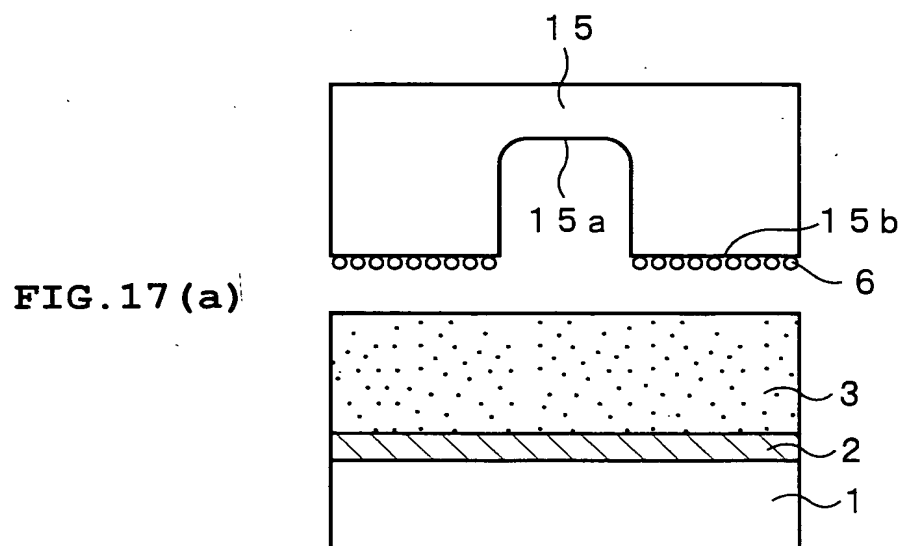


FIG. 18

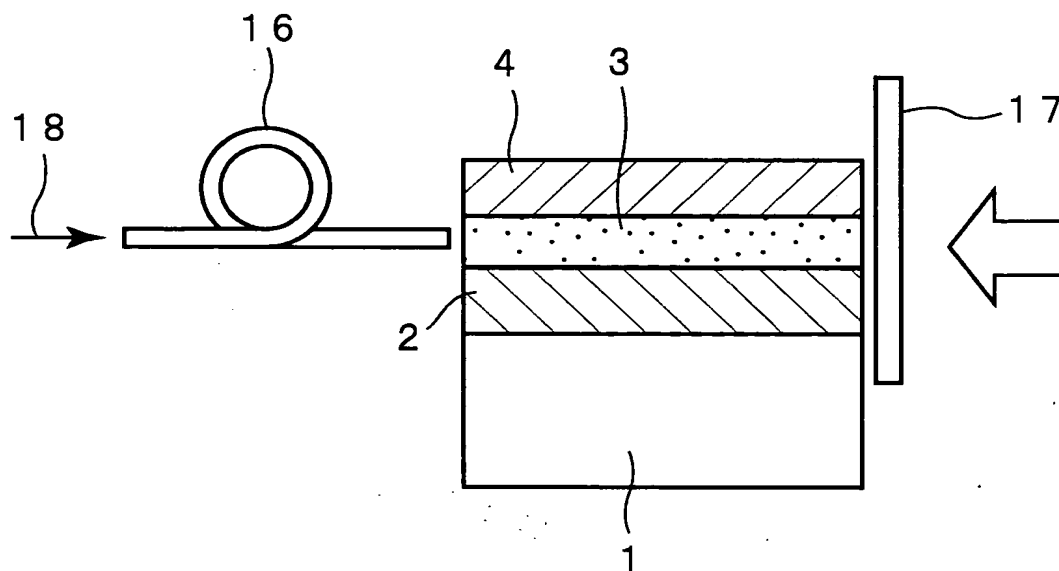


FIG. 19

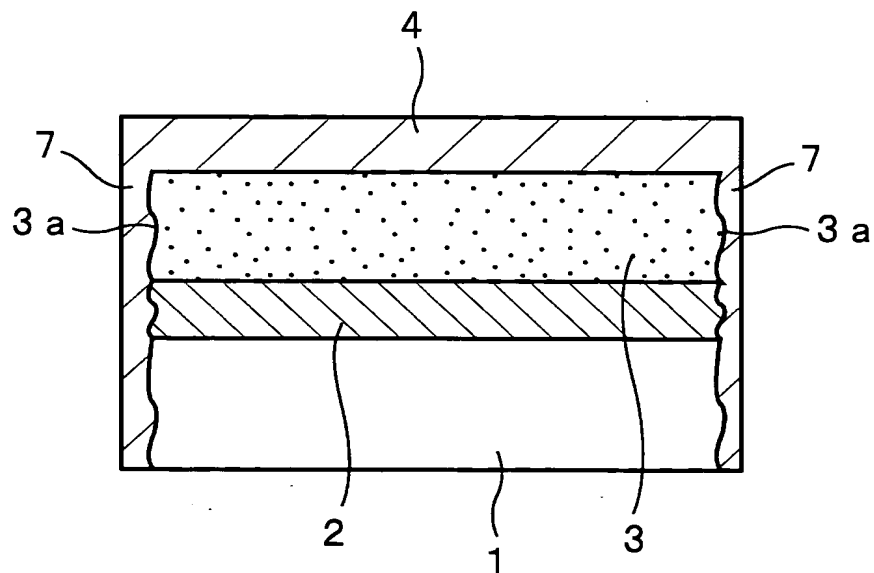


FIG. 20

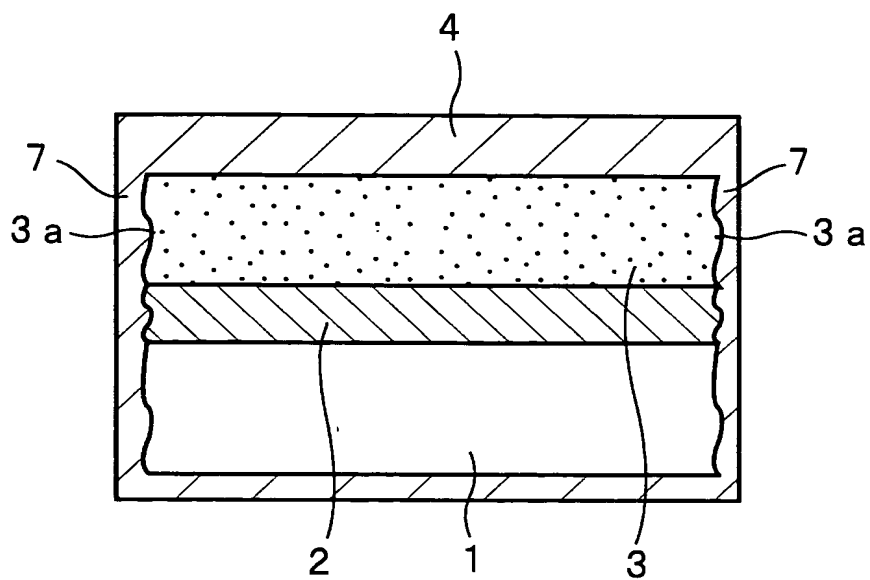


FIG. 21

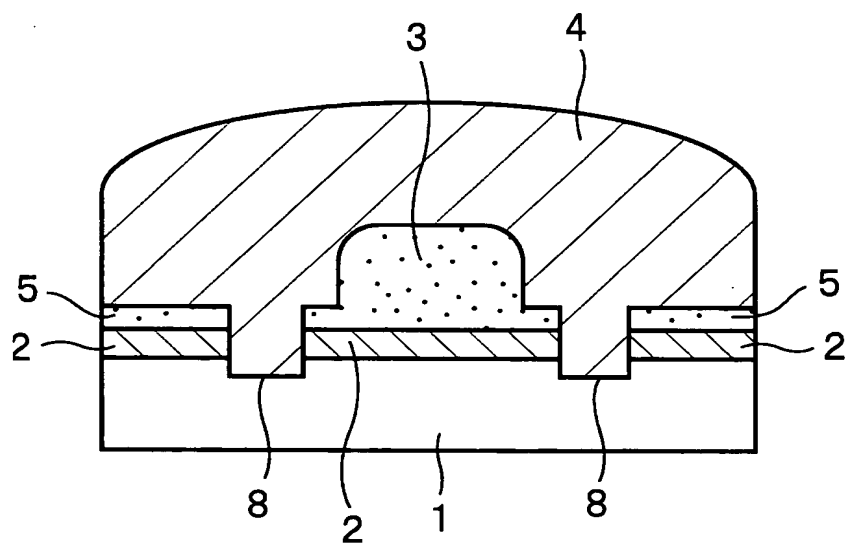


FIG. 22

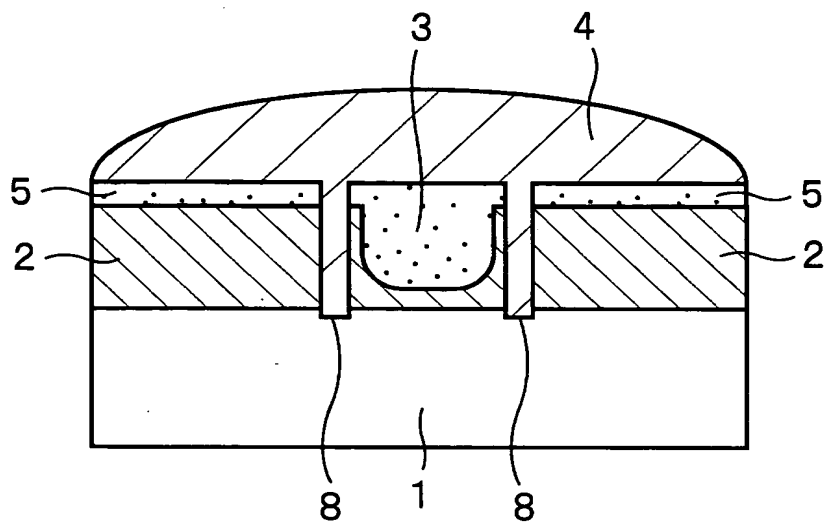


FIG. 23

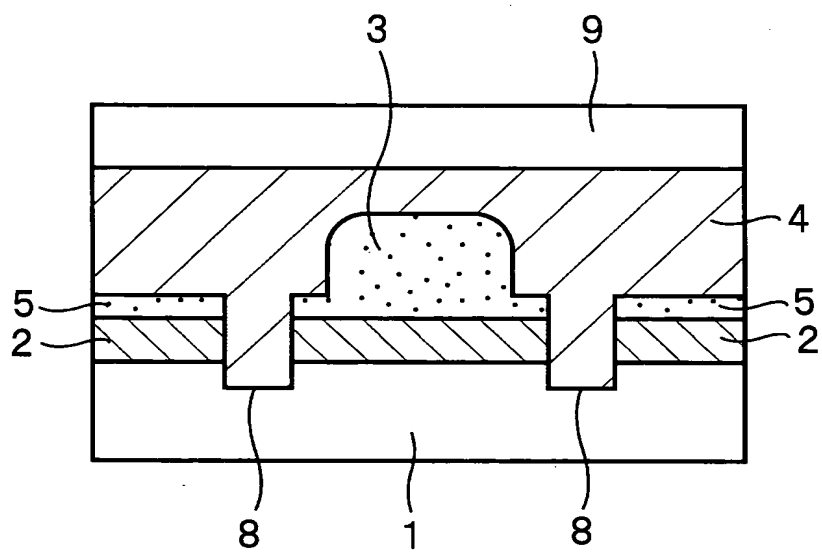


FIG. 24

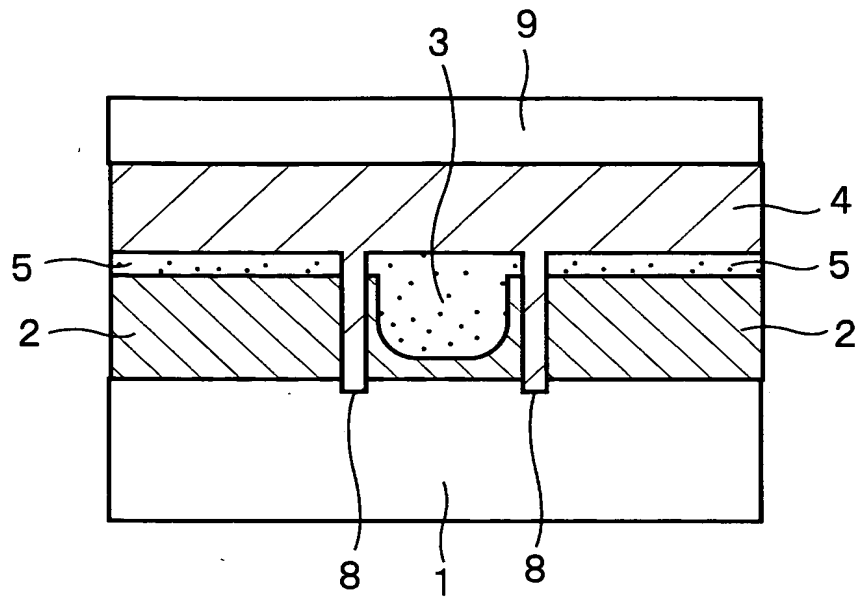


FIG. 25

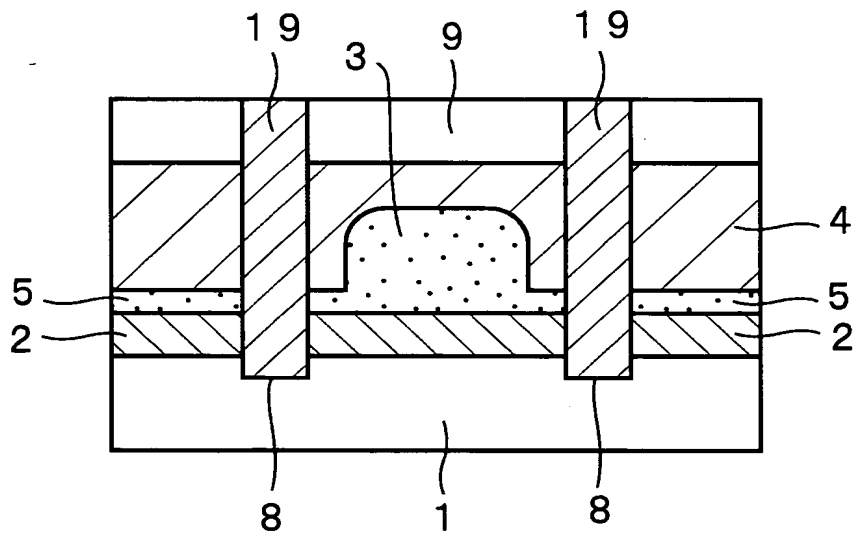


FIG. 26

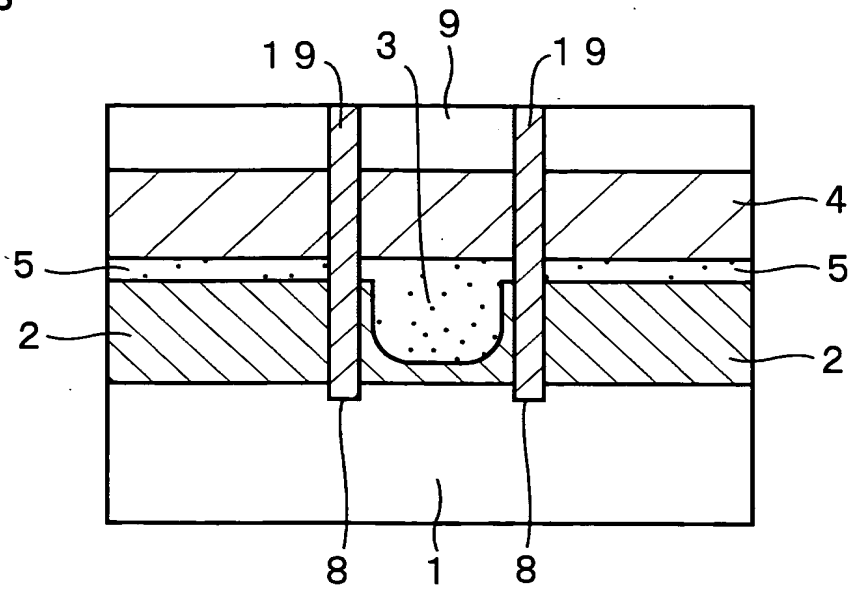


FIG. 27

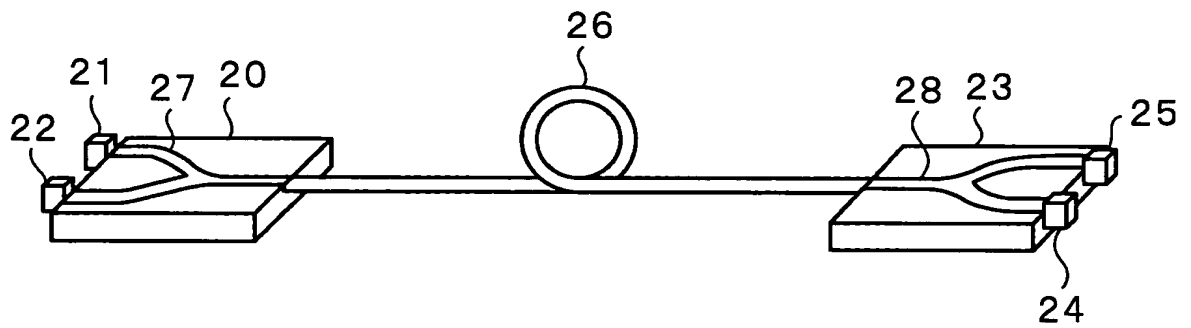


FIG. 28

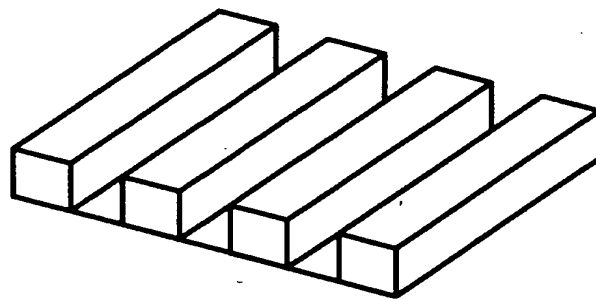


FIG. 29

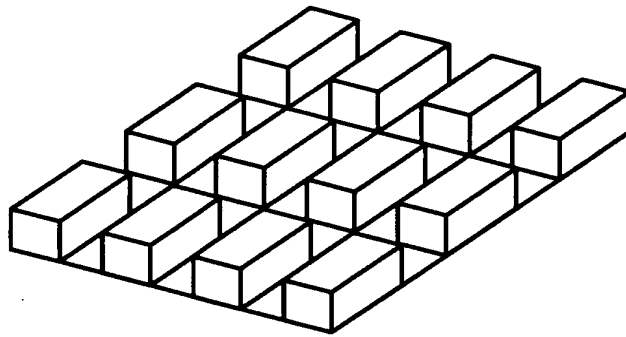


FIG. 30

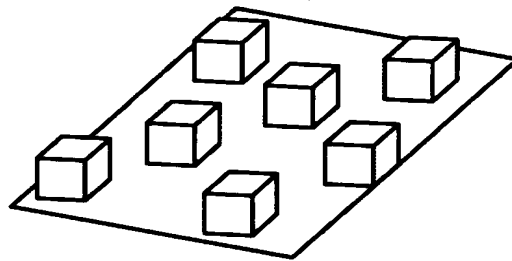


FIG. 31

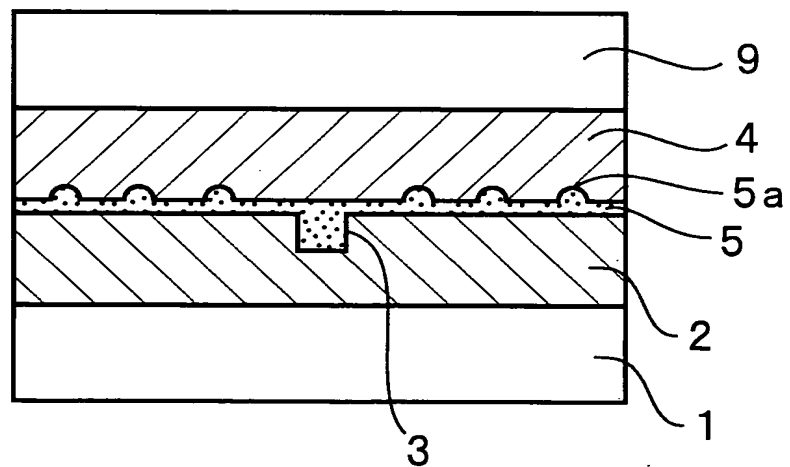


FIG. 32 (a)

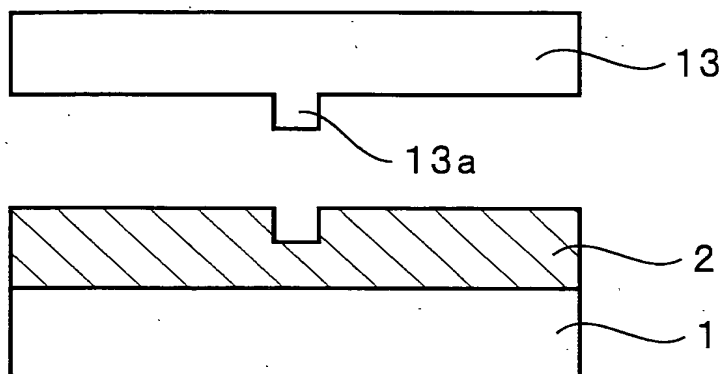


FIG. 32 (b)

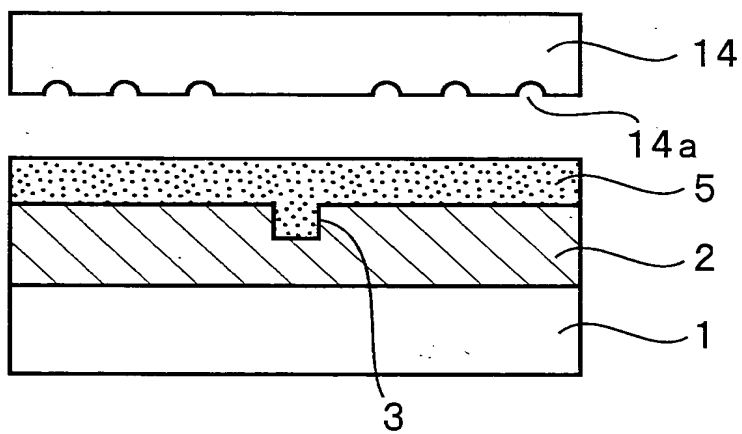


FIG. 33 (a)

FIG. 33 (a) is a cross-sectional view of a semiconductor device. It shows a substrate 1 with a layer 2 on top. Layer 2 has a central rectangular opening 3 filled with a stippled material. Above layer 2 is a thin layer 5, and above that is a layer 5a containing several circular features. The topmost layer is labeled 14.

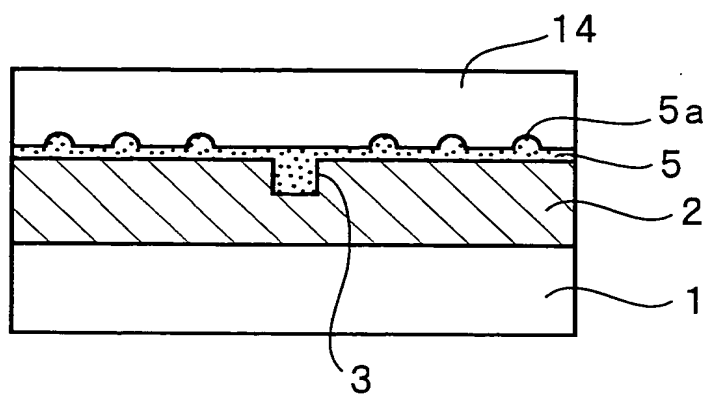


FIG. 33 (b)

FIG. 33 (b) is a cross-sectional view of a device assembly. It shows a substrate 1 with a layer 2 on top. A layer 3 is formed on layer 2, with a rectangular opening 5 in the center. A layer 5a is formed on top of layer 3, filling the opening 5. A layer 14 is formed on top of layer 5a, with a series of semi-circular protrusions 14a along its bottom edge.

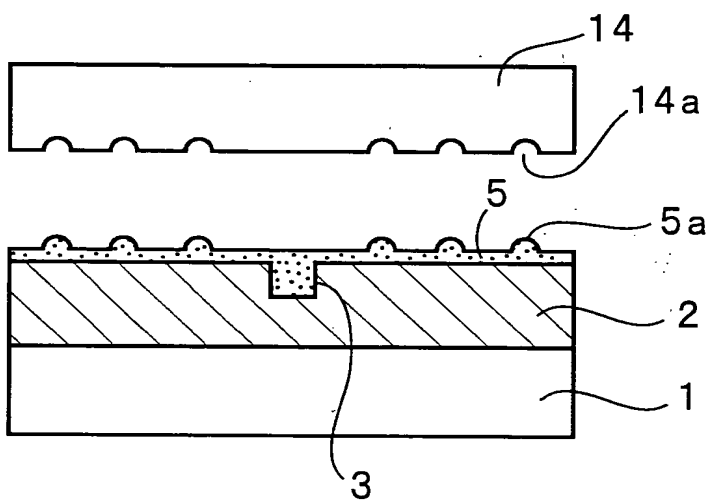


FIG. 33(c)

FIG. 33(c) is a cross-sectional view of a device. It shows a substrate 1 with a layer 2 on top. Layer 2 contains a central region 3 filled with a dotted pattern. Above region 3 is a layer 5, which has a series of small, rounded protrusions 5a on its top surface. Layer 5 is covered by a hatched layer 4, which is in turn covered by a top layer 9.

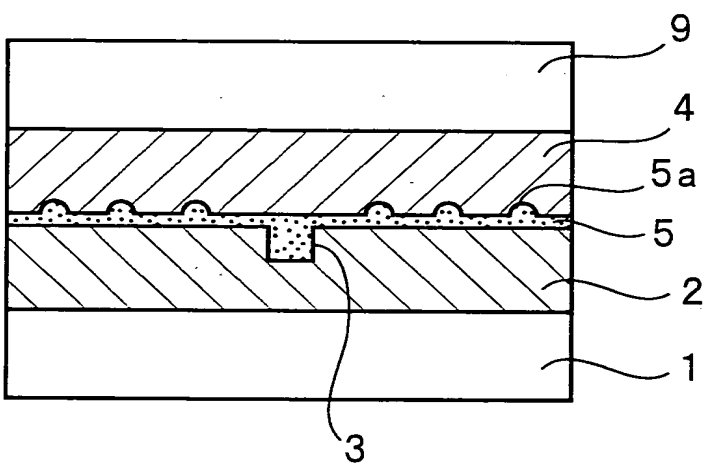


FIG. 34

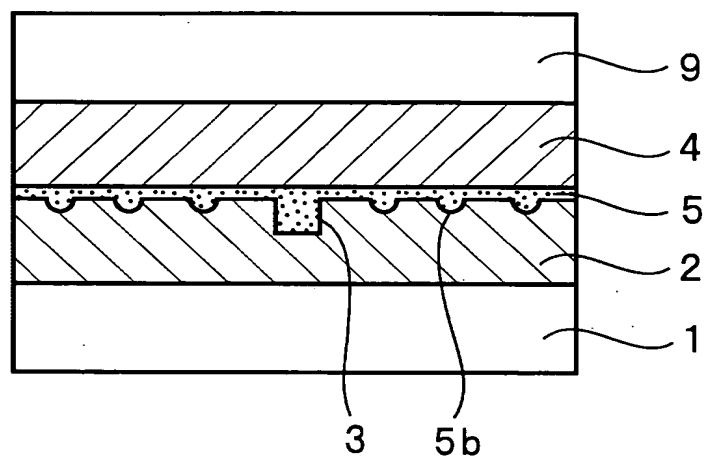


FIG. 35

